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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,883	03/27/2006	Winifried Jansen	DE03 0007.US	6208
65913	7590	07/02/2007	EXAMINER	
NXP, B.V.			FUTEL, GAYLA S	
NXP INTELLECTUAL PROPERTY DEPARTMENT			ART UNIT	PAPER NUMBER
M/S41-SJ				2609
1109 MCKAY DRIVE				
SAN JOSE, CA 95131				
			NOTIFICATION DATE	DELIVERY MODE
			07/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)
	10/541,883	JANSEN, WINIFRIED
	Examiner Gayla Futel	Art Unit 2609

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,3-5 and 7 is/are rejected.
- 7) Claim(s) 2 and 6 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 07/07/2005.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, and 5 rejected under 35 U.S.C. 102(e) as being anticipated by Mohindra (US Patent No. 6,721,548).

3. Regarding claims 1 and 5, Mohindra et al. teaches a method and circuit arrangement for determining the signal strength in a receiver or transmitter with complex signal processing using the in-phase channel (I-channel) and the quadrature channel (Q-channel, characterized in that an evaluation unit is provided which has two inputs (**Fig. 1, #20**) for the field strength signals of the I-channel and of the Q-channel and which generates an overall field strength signal on a logarithmic scale (**Col. 3, line 65-Col. 4, line 4**) without intermediate frequency residues from the individual field strength signals (**Col. 3, lines 22-25**), in order to output it at an output of the evaluation unit (**Fig. 1, RSSI**).

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4. Regarding claim 3, Mohindra et al. teaches the method of claim 1 as stated above. Mohindra et al. further teaches the field strength signals of the I-channel and of the Q-channel are fed to the evaluation unit (**Fig. 1, #20**) without amplification (**Fig. 1**).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mohindra et al. (US Patent No. 6,721,548) in view of Mohindra (US Patent No. 6,442,380).
Mohindra et al. teaches the method of claim 1 as stated above. However, Mohindra et al. fails to teach the field strength signals of the I-channel and of the Q-channel are amplified before they are fed to the evaluation unit. Mohindra teaches a transceiver with a RSSI (**Col. 4, line 51-55**) in which the field strength signals are amplified by zero-IF amplifiers (**Fig. 1, #23, 24**) prior to those signals reaching the RSSI. It would have been obvious to one of ordinary skill in the art to amplify the field strength signals prior to feeding them to the evaluation unit because the gain of the amplifiers can be controlled and would make it easier to reduce the error in the overall field strength signal.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mohindra et al. (US Patent No. 6,721,548) in view of Garskamp (US Patent No. 4,972,512).

Mohindra et al. teaches the circuit arrangement of claim 1 as stated above. However, Mohindra et al. fails to teach that the evaluation unit contains in each case one diode for the I-channel and the Q-channel, where the anodes of the diodes are in each case connected to the inputs for the field strength signals of the I-channel and of the Q-channel and the cathodes of the diodes are connected to one another, to a current source and to the output of the evaluation unit. Garskamp teaches a logarithmic amplifier circuit (**Fig. 1**) with a cascade of limiting amplifiers (**Fig. 1, A1 to A5**) that are coupled to the anode of diode elements (**Fig. 1, D1 to D5**). The cathodes of the diode elements are connected to a summer (**Fig. 1, S**), which outputs a logarithmic signal (**Col. 4, lines 37-40**). The logarithmic signal is then fed into an antilog circuit and produces an output signal (**Fig. 1, #20**). It would have been obvious to one of ordinary skill in the art to replace the ABS of each channel, summer, and logarithmic signal former of Mohindra et al. with the logarithmic amplifier circuit of Garskamp because the output signal can be at an optimum linearization value. The ABS of each channel can be replaced with the limiting amplifier and a diode from Garskamp. Garskamp's logarithmic amplifier can have as many or as few limiting amplifiers as desired. The same adder can be used for each channel to reduce the number of components needed in the circuit. By doing so, the cathodes of the I-channel and the Q-channel are connected to each other. The summer outputs the logarithmic signal (**Col. 4, lines 19-22**) to the antilog circuit. The output of the antilog circuit is the output of the evaluation unit. The detail of the antilog circuit (**Fig. 5**) shows a current source coupled to a transistor. Since the base of the antilog circuit is the logarithmic signal, the cathodes of

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the diodes from the I-channel and the Q-channel are coupled to the current source (**Fig. 5, 19'**) and the output of the evaluation unit (**Fig. 5, V_o**).

Allowable Subject Matter

8. Claims 2 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Moloudi et al. (US Patent No. 6,417,737)
- Wilson (US Patent No. 5,627,857)
- Darabi (US PG Publication No. 2003/0181179)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gayla Futel whose telephone number is 571-270-3008. The examiner can normally be reached on Mon-Thur 7:00 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GF


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